In the Abstract:

Delete the existing Abstract, and substitute the following in its place:

A method of fabricating integrated circuitry includes forming a conductive line having opposing sidewalls over a semiconductor substrate, and having an outer etch stop cap. An insulating layer is deposited over the substrate and the line. The insulating layer is planarize polished using the outer etch stop cap as an etch stop. After the planarize polishing, the insulating layer is etched proximate the line along at least a portion of at least one sidewall of the line. After the etching, an insulating spacer forming layer is deposited over the substrate and the line, and it is anisotropically etched to form an insulating sidewall spacer along said portion of the at least one sidewall.